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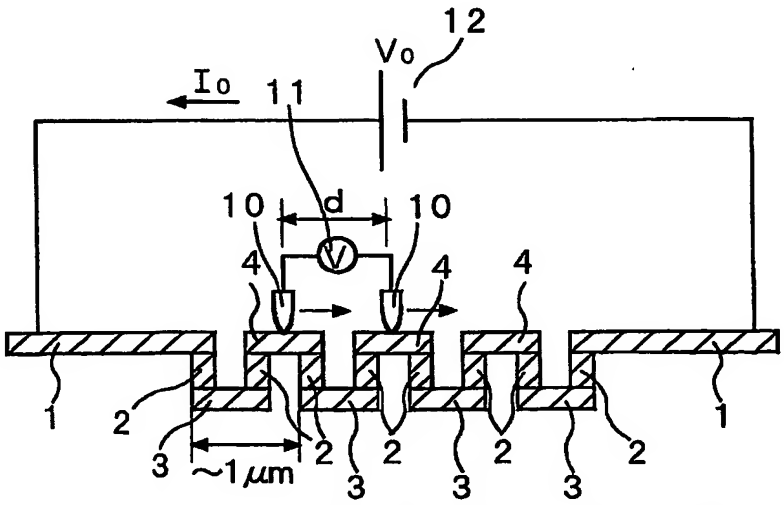

(57) Abstract: A pair of pads (1) are formed on an insulating layer formed on a top surface of a substrate, and a plurality of through- holes (2) are arrangedlaid out at equal intervalsintervals between the pads (1). The adjoining through holes (2) are connected alternately by upper-layer wireupper interconnect lines (4) exposed on the insulating layer or lower-layer wirelower interconnect lines (3) buried in the insulating layer, thus constituting a check pattern. A DC power supply (12) is connected between the pair of pads (1), and a constant current Io is supplied to a chain pattern of the through holes (2). Two probes (10) move on a chip surface along the chain pattern of the through holes (2) while keeping a given intervalspacing d. Accordingly, the probes (10) sequentially scan the upper-layer wireupper interconnect lines (4) exposed through the chip surface of the chain pattern of the through- holes (2).

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